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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Leonard Forbes et al.

Title: TRANSISTOR WITH VARIABLE ELECTRON AFFINITY GATE AND METHODS OF FABRICATION AND USE

Docket No.: 303.324US2

Serial No.: 09/256,643

Filed: February 23, 1999

Due Date: November 13, 2002

Examiner: Michael Trinh

Group Art Unit: 2822

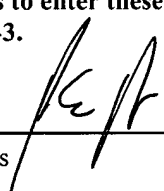
Commissioner for Patents
Washington, D.C. 20231

We are transmitting herewith the following attached items (as indicated with an "X"):

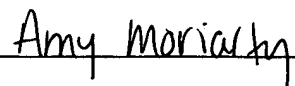
- ☒ A return postcard.
- ☒ A Response under 37 CFR § 1.111 (6 Pages).
- ☒ A Supplemental Information Disclosure Statement (1 pg.), Form 1449 (2 pgs.), and copies of 72 cited references.
- ☒ A check in the amount of \$180.00 to cover the fee for consideration of Information Disclosure Statement under 97(c).

Please consider this a **PETITION FOR EXTENSION OF TIME** for sufficient number of months to enter these papers and please charge any additional required fees or credit overpayment to Deposit Account No. 19-0743.

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.
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By: 
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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Commissioner for Patents, Washington, D.C. 20231, on this 13th day of November, 2002.

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